XRM2-ADC-D2/125 User Manual

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ALPHA DATA

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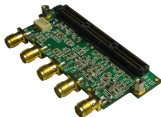
1 Introduction

Figure 1 : XRM2-ADC-D2/125

The XRM2-ADC-D2/125 is a front panel adapter card designed for use with Alpha Data's FPGA-based XMC and VPX cards.

The XRM2-ADC-D2/125 provides two channels of analogue to digital conversion with 14 bit resolution and supports sampling rates up to 125 MHz It is aimed at applications such as IF/Baseband Signal Sampling.

A number of customisation options are offered with this card, ranging from signal input connector style through to transformer or DC- coupling of inputs.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock.

Two auxiliary I/O ports are provided for use as trigger inputs and general purpose signalling.
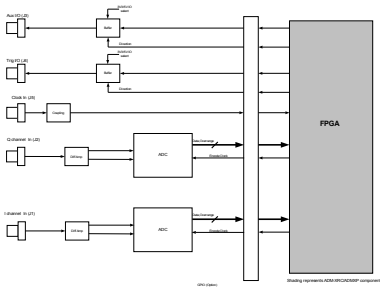

Figure 2 : XRM Block Diagram

2 Installation

The XRM2-ADC-D2/125 is designed to plug in to the front panel connector (SAMTEC QSH series) of the XRC series of cards. The retaining screws should be tightened to secure the XRM2-ADC-D2/125.

> **Note:**
> This operation should not be performed while the PMC card is powered up.

2.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

Avoid flexing the board.

3 Specification

3.1 Inputs

3.1.1 I Signal (J1), Q Signal (J2)

Input:	50 Ohms
Bandwidth:	10 Hz to 200 MHz
Level:	±1V = ADC Full Scale

There is a DC Coupling manufacturing option. Contact the factory for further details.

> **Note:**
> exceeding the maximum limit may result in permanent degradation of converter performance.

3.1.2 Clock In (J5)

Input:	50 Ohms, ac coupled
Level:	0 dBm nominal

> **Note:**
> exceeding the maximum voltage limit may result in permanent degradation of converter performance.

3.2 Input /Output

3.2.1 Trig IO Port (J4)

User configurable as input or output

Input:	4k7 Ohms, dc coupled
Level:	+3V3 LVTTL or +5V TTL (factory/user selectable [1])

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[1] - configured via 0R links

3.2.2 Aux. IO Port (J3)

User configurable as input or output, direct to FPGA pins.

Input:	4k7 Ohms, dc coupled
Level:	+3V3 LVTTL

4 Options

4.1 Connector type

- SMA (7 mm, standard)
- Long Barrel SMA (20 mm)
- SMB
- SMC

4.2 Sample Rate

1MHz to 125MHz

4.3 Order Code

XRM2-ADC-D2/125[Connector option][IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option. For custom filter designs or other customisation requirements (e.g. connectors) please contact Alpha Data.

5 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

> **Note:**
> This product requires an export licences for companies outwith EU, Australia, Canada, Japan, New Zealand,
> Norway, Switzerland or the USA. Contact the factory for further information.
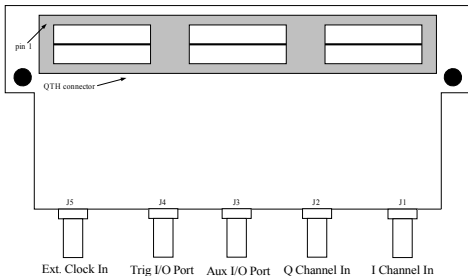
6 Board Layout

pin 1

QTH connector

J5	J4	J3	J2	J1
Ext. Clock In	Trig I/O Port	Aux I/O Port	Q Channel In	I Channel In

Figure 3 : XRM2-ADC-D2/125 Board Layout

Note:
This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

Revision History

Date	Revision	Nature of Change
Feb 2019	1.0	First issue

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